

# computer designer's handbook

## DESIGN OF AN INTEGRATED SUBMICROSECOND CORE MEMORY

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Here's how the change in memory system organization and design criteria produced by rapid advances in monolithic circuit technology has been applied to a modular submicrosecond computer main memory — the ICM-40.

High-speed random access storage capability accounts for a significant portion of the hardware volume and cost of computing systems of all sizes. Advances in the state of the art in combination with cost/performance improvement have expanded applications requiring and justifying large capacity high-speed storage. Application of computers to large and small scale real-time problems has accentuated the need to expand high-speed memory capacity as opposed to slower, less costly competing forms of storage.

Expansion of installed ferrite core memory capacity in recent years is a classic example of price/volume interaction in the marketplace. As the cost of a given function or capability decreases, or as a price/performance ratio becomes more favorable, the number of requirements to which a given technology is applicable increases accordingly.

Application of monolithic integrated circuits to high-speed ferrite core memories significantly improves price-performance ratio for this type of storage, and extends the spectrum of applications available to the product.

### Product Concept

The ICM-40 was designed to satisfy a range of memory system requirements in the 100K to 1.5M bit storage capacity range. Desired usability in a proposed new generation of computers with salability as a general-purpose system component dictated modular expandability in data word length and in address capacity. Application to such a wide range of storage capacities and different requirements presented an engineering challenge and necessitated special consideration in electrical and mechanical design to achieve performance and cost objectives. Design objectives were to achieve a cycle less than 1  $\mu$ sec, with less than 500 ns access time, and to provide an enhanced product lifetime and cost/performance potential by maximizing application of integrated circuits.



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Mr. Reichard coordinates activities of magnetic core memories, specializing in circuit and system design and development of complex memory systems. He received his BSEE and MSEE degrees from Massachusetts Institute of Technology.

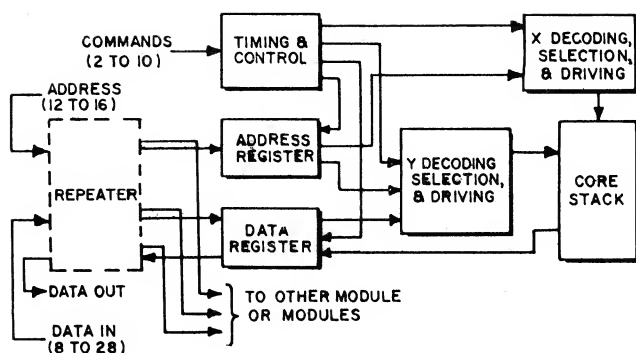


Fig 1 — ICM-40 System Block Diagram

## Program Concept

Return on investment is far from a new term in the accounting world, but only in recent years have intensified competitive pressures resulted in detailed consideration of this factor in engineering management. Return on investment — in the engineering sense — is maximized by optimum resolution of contradictory objectives:

- Maximize product lifetime and sales volume.
- Minimize development time and cost.
- Maximize use of knowledge and techniques from other development programs and commonality of design and components with other company product lines.
- Achieve a balanced risk program and engineering design — one without overwhelming dependence on a potential technological breakthrough.
- Capitalize on technical innovation and advances by bringing them to market in the shortest possible time.

**Product Lifetime** — Lifetime and total dollar volume, achievable by a product design, are primarily functions of its competitive performance and price position (neglecting available market size and manufacturing capacity limitations). You must consider initial position, at time of product introduction, and improvement potential — presently achieved in EDP equipment by extensive use of integrated circuits.

**Development Time and Cost** — You usually minimize the development investment at the expense of an extended product lifetime, since it is relatively easy to “brute force” a given performance capability or achieve it at non-competitive cost levels. A product which achieves high performance and relatively low cost through sophisticated simplicity of design offers longer lifetime and better competitive position. To reduce investment, carefully time development programs to take advantage of technological breakthroughs and new components without markedly increasing risk levels, and evaluate and communicate end product performance objectives prior to the program, plan carefully, monitor performance, and correct action as problems occur. Low risk engineering programs which may result in only marginal product improvement or “upgrading” are usually costly, and a poor choice from a return on investment point of view despite their short-term attractiveness. In summary, it is meaningful to talk about minimization of the development investment only at or above a critical risk level — that level high enough to ensure reasonable product lifetime. Proper resolution of the cost-risk conflict leads to determination of engineering program objectives which are difficult but reasonable.

**Design Commonality** — Objectives of an engineering program cannot be determined independently of general business plans. Potential advantages of standardization and multiple application of experience, knowledge and techniques in conservation of engineering resources are great. Monolithic integrated circuits offer new leverage in realization of these advantages, but also require reconsideration of approaches previously devised from discrete component system design criteria. A factor in formulation of ICM-40 development plans was the utilization of existing integrated circuit and module development, and of in-house circuit design and fabrication capability to produce proprietary circuits resulting in superior performance. Thus, mechanical packaging, from the basic card module up to final assembly, uses hardware common to the “micropack” ( $\mu$ -PAC) product line.

**Capitalize on Innovation** — Competitive position and product lifetime are greatly enhanced by timeliness of introduction to the market. The designer who is first to apply an innovation or advance in technology to a given product area or function obtains an advantage not easily overcome by competition which can only say “me too.” For instance, the term “integrated circuit computer” has been applied to a machine in which the “integrator” was limited to a few circuit cards of integrated registers. This may solve an advertising problem, but the ultimate cost/performance advantages of integration accrues only to a machine in which this technology is massively employed in all subsystems, including core storage.

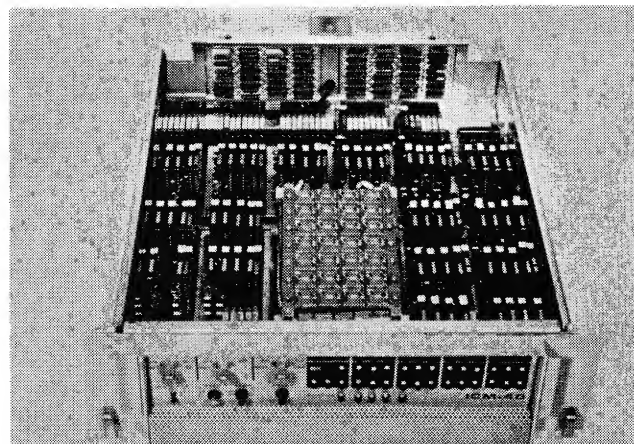


Fig 2 — 8192-Word, 28-Bit ICM-40 Memory System

**Risk Balance** — Engineers generally operate within a hierarchy of risk decisions. The highest level is the basic feasibility of a product or performance capability. Once an affirmative decision has been made at the feasibility level, another entirely new level comes into play — the “approach” level, and this process repeats as decisions are made at successively lower levels. The most important decision criterion at the approach level devises a program which achieves reasonable risk balance, one in which achievement of goals does not depend upon a potential — as yet unrealized — technological breakthrough. This risk balancing process is analogous to organization of a PERT plan to minimize length of the critical path and slack in subsidiary paths. For example, once the decision to utilize integrated technology is made, the next question is “to what extent?” For the ICM-40 the decision was *not* to attempt development of an integrated core driver because this approach constituted a risk unbalance in the temporal and financial context of the program.

## Core Memory Technical and Market Trends

Since 1952 the most common form of high-speed random access digital storage has been the ferrite core memory. The storage capacities most frequently used over this period of years have increased from tens of thousands to millions of bits. Address access cycle times have been decreased from 20  $\mu$ sec to less than 1  $\mu$ sec. Power consumption and physical size have been reduced by the same order of magnitude. Along with advances in performance, a continuing downward trend in costs has expanded applications in digital systems. This trend has brought a large number of manufacturers into the memory system business and produced intense competition. Since memories are a very significant portion of computer hardware costs, manufacturers must compete in this market as well. Rapid technological advances in electronics and continuing improvement in ferrite core performance and uniformity compound the situation. Intense competition and rapid technological advances have made difficult the selection and execution of a development program aimed at a manufacturable product with a reasonable product and profit life. In general, recent history leads one to the conclusion that a good memory system design offered at the appropriate time will be obsoleted in 2 to 4 years by a superior design offering better performance for a lower price.

### Program Definition

**Electronics** — Application of integrated circuits in memory design profoundly affects memory system organization. Coupled with this effect is the ever-present demand for decreased cycle time. Memory input-output interface and logic functions can be easily implemented from standard integrated logic circuits. Furthermore, it becomes economically feasible to employ more gates and flip-flops than justified when you are using discrete circuits. In addition to present cost considerations, the rate of decrease in the cost of monolithic integrated circuits will be very high. The result of these considerations in memory system design is that you can make extensive and redundant use of logic functions without penalty in overall design cost.

Ferrite core stack drive and sensing circuitry present a problem distinct from the logic functions. Basic considerations here are impedance and signal level transformation from the decoding functions to drive the core array and to sense its output signals. In the case of direct stack driving circuitry, the problems of high voltage and power dissipation challenge the present state of the art of monolithic integrated circuit development. Although the eventual integration of these circuit functions is desirable, a practical approach is the discrete drive matrix used in the ICM-40. Sensing circuitry, however, makes lesser demands on present monolithic integrated circuit techniques and is available for practical application in product designs. The production level of these devices, will be substantially lower than the more common logic circuits.

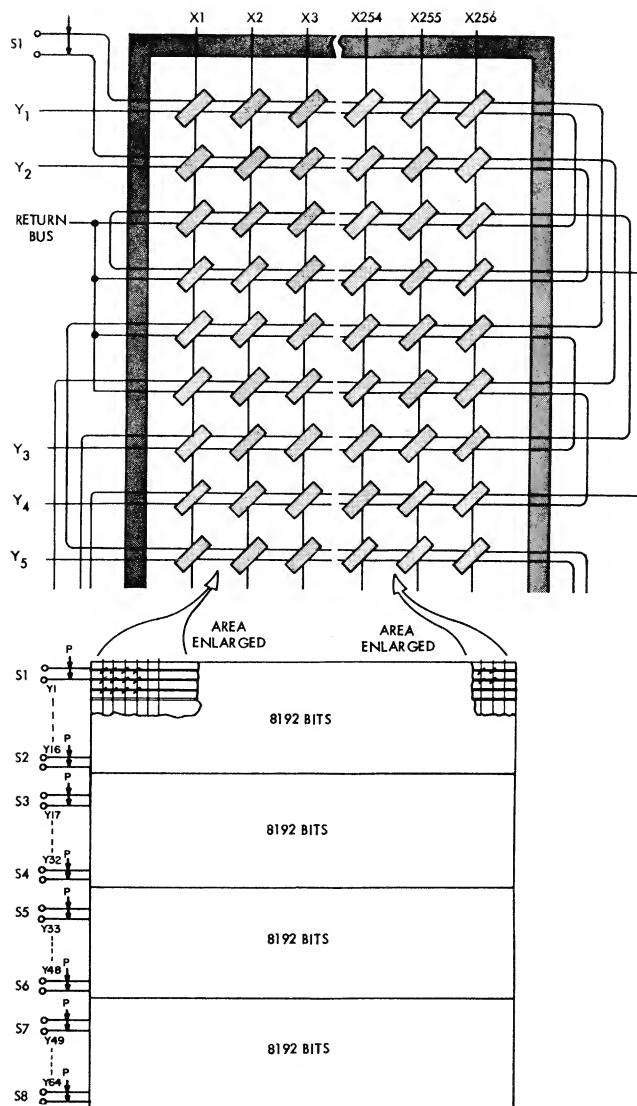


Fig. 3 — Each plane contains four identical areas, in each two longitudinal sense windings are interlaced. Each area contains 256 rows of 32 cores. X drive lines pass through all planes in the conventional manner, threading a maximum of 896 cores, only 16 of which are linked by a single sense winding. Y drive lines are contained within individual planes and thread 512 cores of which half are linked by one sense winding. By staggering the drive currents the sense amplifier is subjected to the disturb signal of only 8 delta-pairs.

**Ferrite Core Technology and Memory Arrays** — Trend in ferrite core design has been to smaller diameters which provide faster switching times. An additional advantage of a smaller core is higher packing density, reducing the line lengths for drive and sense thus improving the electrical characteristics of the array for higher speed operation. As the core diameter decreases, the stringing and stack assembly problem increases. It is desirable therefore to decrease the number of wires passing through each core and to develop techniques which minimize cycle time limitation imposed by a given core diameter and switching time. The present means of assembly is mostly manual; consequently, the core diameter and number of wires is important in determining assembly cost. Designing for the largest diameter core practical for the required memory system extracts the optimum performance from the ferrite core array by considering switching time, required drive current and packing density. In any case, presently available ferrite cores offer sufficiently

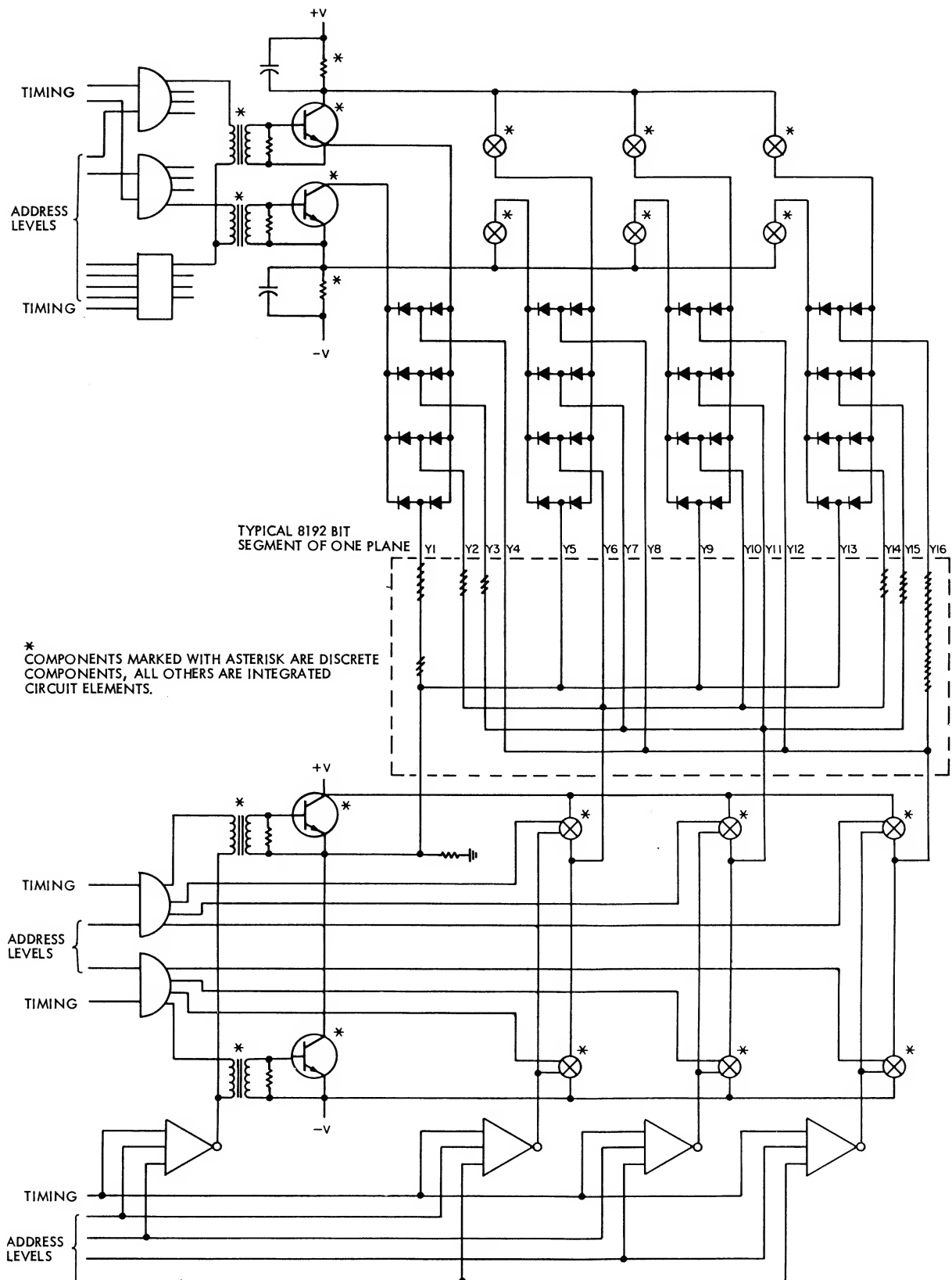


Fig 4 — The driving matrix consists of direct-driven double-ended (switch and sink) matrices in each coordinate, with two diodes per line and a stack-discharge or reference resistor on each sink bus. The switches and sinks are transformer-driven. There is no current-driver; the switches are uniform in turn-on so that no variance in peaking time may be observed. Precision resistors and a regulated floating supply determine current.

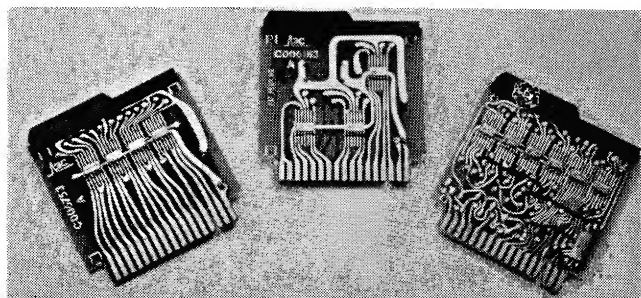
uniform characteristics and fast switching time to ease selection through the use of coincident current technique.

**Storage Array/Electronic Cost Ratio and Interactions** — From the time of the first ferrite core memories to the present, the most economical and therefore the most popular organizational structure has been the 4 wire coincident current array. Linear select (word organized) or other configurations replaced this structure only when dictated by extremely short cycle times or other special requirements. The cost of the storage array and the cost of the necessary control, selection, drive and sense electronics determine the economics of any given system. You must consider this with performance, the standards of which are set by surrounding logic circuits and the required memory cycle time to allow operation of the logic circuits at optimum speed in a digital computer. It is evident that you can achieve a given cost level by cost tradeoffs or allocations to each of these areas. In making the design decisions which affect this tradeoff, you should consider projected future cost trends over the anticipated product lifetime as well as present-day cost levels.

It is our opinion that the technology of ferrite core storage devices and arrays is a relatively mature one, and offers significantly less potential for cost reduction than that of monolithic integrated circuits. The design of the ICM-40 memory therefore allocates a relatively higher portion of total system cost to electronics and emphasizes reduction of storage array contribution to a minimum.

## Technical Approach

Advantages of a magnetic storage element having a closed path (lack of creep, high signal-to-noise ratio, insensitivity to external fields, high energy efficiency and relatively simple mechanical considerations) need no elaboration here; the choice is clear. Having chosen core arrays as storage medium, we must minimize this portion of system cost. It has been accepted that the fourth wire of the "3D" coincident-current array incurs a disproportionate portion of the cost of threading an array. As the 3-wire ICM-40 stack is contrasted to a conventional stack, the eliminated wire is the inhibit wire. This is done by replicating one coordinate of current source for each bit, in a technique described in the literature several years ago, but only recently made economically feasible by the



**Fig 5** — System electronics, predominantly integrated circuits are contained on etched circuit modules and inserted into connectors and hardware (standard equipment 3C's  $\mu$ -PAC line.)

advent of integrated circuits. Other factors in reducing the effective core stack cost include minimization of external wiring by incorporating diode matrices and by performing a maximum of drive-line bussing directly on the core planes.

An additional technique to reduce total cost is one of using re-entrant lines in one coordinate to achieve reinforcement or cancellation of currents in one of two cores linked as a function of the direction of current relative to that in the other coordinate. This technique is possible because of the short wire length due to the organization of the ICM-40 core stack.

A further advantage of 3-wire core planes is that these are more capable of being extrapolated to smaller cores than a 4-wire stack; hence they may follow the trend toward faster and/or lower-drive cores as the need arises or the market demands.

## System Organization

The basic ICM-40 provides 0.5  $\mu$ sec access time, measured from the input terminals to the output terminals of the system. Wider-than-normal margins, assure cycle time of less than a microsecond. Storage systems, Fig 1, use a basic module, Fig 2, of approximately 230,000 bits, organized either as 16,384 words of 14 bits maximum or as 8192 words of 28 bits maximum. Units of smaller capacity are also economically manufacturable. When either address capacity or word length is increased above these limits, a data repeater is provided so that the controlling equipment communicates with only one specified interface.

The repeater receives incoming data and provides regenerated data over short lines to the appropriate module or modules. This approach allows the individual modules to be mass-produced and tested in a straightforward, repetitive manner capable of highly automated production. The repeater also adapts other than standard logic levels so that such adaption need not be duplicated.

**Storage Array** — The stack uses 3 wires per core, one core per bit, fully switched, in a driving scheme known today as  $2\frac{1}{2}$  D selection. Cores presently used are of 0.030" OD, require a half-drive of about 375 ma, and switch in less than 250 nsec. The requirement for variable word length and capacity in a family of computers as well as for the general purpose market necessitates a modular stack; our solution uses one plane type to provide either 2 bits of 16,384 words or 4 bits of 8192 words. Smaller word capacities require a different type. Up to seven planes may be stacked, corresponding to the module capacities cited, Fig 3.

Line length reduction, due to the stack organization, permits mismatched termination without severe degradation of current wave-forms. This in turn permits lower drive voltage, which not only reduces power consumption but eases the requirements on semiconductor devices in the driving matrix, Fig 4.

**Electronics**—The electronics portion, Fig 5, functionally organized, minimizes the number of circuit module types and simultaneously creates an iterative add-on ability for increasing capacity above the minimum. An 8192/28 unit contains 10 standard logic modules of 5 types and 82 modules of 4 types which are peculiar to memory requirements: 2 address register  $\mu$ -PACs, each with seven dc-gated flip-flop stages, all integrated circuitry; 14 bit-register modules, each containing integrated receivers, gates, flip-flops and sense amplifiers for two bits of 8192 or fewer words; 64 decoding/selection modules of one type and one subtype containing both integrated and discrete



components; and two timing distributors containing integrated and discrete components and lumped-constant delay lines providing control timing.

Three special integrated circuits were developed for the ICM-40, a sense amplifier, a diode matrix and a decoder-driver; each contained in one TO-84 flat pack.

The sense amplifier provides stable and uniform linear differential amplification, signal rectification, threshold discrimination, strobing and pulse-stretching. The first four functions are prerequisites for a sense amplifier in any large size memory system. Pulse-stretching ensures a uniform pulse-width output despite minor variations in gain or threshold, increases the driving capability of the circuit and enables a dot-or connection of outputs which sets the appropriate data register via a single logical input. Use of an integrated-circuit sense amplifier is made possible by a stack organization which provides less than 1.5 v of common-mode noise on a sense winding encompassing 4096 cores.

The diode matrix provides a sixteen-diode array in one TO-84 flat pack. The diodes, 0.5a and 40 v, serve as the usual selection matrix diodes, meeting appropriate specifications on forward drop, reverse leakage, recovery time, etc.

The decoder-driver, Fig 6, provides partial address decoding, control signal gating, and impedance level transformation sufficient to drive a transformer winding. By this means, and by enabling the other ends of the primary transformer windings to pass through standard power gates in a decoding array, an efficient decoder matrix is implemented.

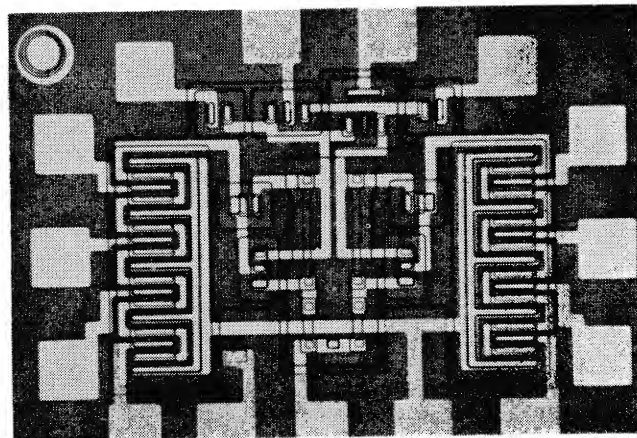
A basic 8192/28 module contains 512 discrete transistors and 512 pulse transformers. All other circuitry is integrated and comprises the following TO-84 flat packs: 56 sense amplifiers, 64 decoder-drivers, 88 diode matrices, 74 quad gates, 155 dual power gates, 2 flip-flops and 3 dual gates. Add-on ability for increasing word length requires, for each additional two bits, 5 circuit modules in an 8192-word module or 8 circuit modules in a 16,384-word module.

**Power Supply** — The power supply is a specially developed unit capable of providing all dc power to a 16,384-word 28-bit memory system, or two modules of memory. It requires only three dc supplies, 6 v, -6 v and a floating 24 v supply. Logic circuits in a module dissipate about 40 w at maximum rate. The selection and drive circuits dissipate another 150 w, of which over 80% is in the current-determining resistors. Simply constructed, with low power output the power supply features turn-on and turn-off sequencing, overvoltage protection, and ac line failure sensing. The last provision includes a fault signal which may be used to gate off commands to memory so that an ac line failure doesn't disturb stored data.

**Mechanical Design** — The mechanical design of the ICM-40 satisfies requirements of simplicity, economy of manufacture and assembly and flexibility. Flexibility allows the unit to be mounted horizontally in a RETMA rack for small to medium capacities, or vertically in a special carriage. The 5¼" high unit shares fabricated parts, chassis, cooling units, wiring planes, etc., with the standard 3C  $\mu$ -BLOC enclosures and with the DDP-124 computer.

Cooling units provide forced-air cooling sufficient for reliable operation over an ambient temperature range of 0 to 50 C; two identical cooling units on front and rear of a horizontal unit or top and bottom of a vertical unit provide push-pull forced-air cooling.

**Interconnection** — Interconnection problems of the integrated circuit system have been solved by functional organization and automatic solderless wrap methods. The basic unit is a connector which accepts eight  $\mu$ -PACs each having 34 pins. Each pin has a precious-metal contact for edge-connector pc cards and a rectangular extension which accepts up to three wrapped connections. Each connector incorporates a pair of locating holes so that



**Fig 6 — The TO-84 flat pack includes two circuits, and provides a decoder element with eight outputs which serve to drive primary windings of the selection transformer matrix.**

36 connectors can be simultaneously fixtured for wrapping a grid of 10,368 pins or 288 module locations. In a maximum capacity memory module, approximately 1500 wires are applied automatically to the wrap plane assembly. An additional 500 leads for the core stack, 60 leads for the current-determining resistors, and 50 for bypass modules and other miscellany are manually applied. Note: of the 1300 cu in available in the basic module, about 130 cu in or 10% are used for interconnections.

## Performance Summary

The original performance objectives set for the ICM-40, considered to be difficult but achievable, have been met. These included single module cycle time capability of less than 900 nsec and access time less than 450 nsec with drive-current margins of at least  $\pm 10\%$  in worst-case pattern at maximum rate. The strobe window, or range of adjustment, is limited more by variability of delay in the differential sense amplifier and strobe amplifier than by noise signals or by any propagation delays in drive lines or sense windings.

The final system design includes fewer modules, types of modules and wired interconnections than the original design indicated. Tangible results of this design are reflected in reduced costs of wiring, circuit module testing and system checkout as well as manufacturing and inventory costs.

## Trends in Memory Design

- With the advance of integrated circuits, the decrease in core size, and the need for faster cycle times, core memory organizations and mechanical structures will become more modular.

- Due to the decreasing cost of electronics, it is economically feasible to provide the addressing and address decoding functions to a smaller core matrix and repeat these functions to offer larger capacity memories.

- It is important to limit the drive line lengths to obviate termination reducing power consumption and the compliance voltage level required for drive currents, thus offering a significant saving in cost of electronic circuitry. As cycle times decrease, it is necessary to limit drive line length to prevent excessive delays. It is important to minimize delays from selection, drive and sense on a per bit basis.

- Short drive and sense lines, high bit density storage arrays and repeated electronics make possible small high performance memory modules that can be combined for large memory requirements. Such an approach offers the

memory manufacturer the economics of more uniform and larger scale production. It should minimize manual assembly and test problems since you can assemble the circuitry on pc boards that serve as the supporting frame for the array.

The advantages of magnetic storage elements with lower coercivity than the presently available ferrite cores are obvious. Furthermore, reduced output sense signal amplitudes may be tolerated due to the lower costs incurred in integrated amplifiers. It is meaningless to consider such elements, however, without regard for their cost/performance characteristics. To date, ferrite core arrays offer the best practical solution to digital computer data storage requirements. This has been made possible by the reduction in core size, increased bit density packaging, increased speed of operation, significantly improved uniformity, and a continuing decrease in cost. • •





# H O N E Y W E L L

I N C.

Dear SID Member:

As a member of the display community, we believe that the attached technical article and brochure will be of interest to you. The enclosed literature describes a high-speed core memory which has been used in several state-of-the-art display systems. Typical systems include: Airline Reservation Displays, Television Screen Displays, and CRT Displays.

Some of the features of our memory systems which have enhanced their use in display systems are:

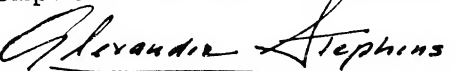
- A fast cycle time (750 nanoseconds to 1.0 microseconds) which permits rapid scan rates, a large number of character positions, and minimization of flicker.
- Several alternative modes of operation (random access and sequential access) which permit the memory to be efficiently used for both character generation and input/output buffering.
- Storage capacity of 4,096 to 49,152 characters in 10-1/2" of panel height, minimizing physical size of the display system.
- Provision for manual insertion of data which allows displayed data to be modified by either the operator, the control system, or maintenance personnel.

If, after reviewing the enclosed literature, you desire additional information, please fill out the self-addressed card or contact our nearest sales office.

Sincerely,

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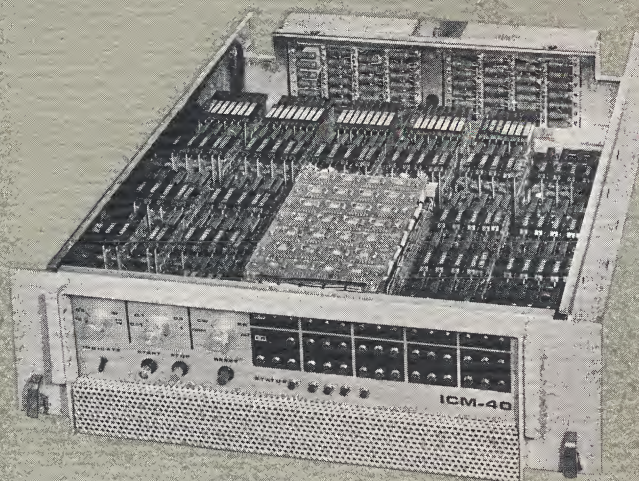


INTEGRATED CIRCUIT  
MAGNETIC CORE MEMORIES SERIES ICM-40





**SERIES ICM-40**  
**integrated circuit**  
**magnetic core memories**



**standard features:**

- 1  $\mu$ sec full cycle
- Monolithic integrated circuitry
- Almost  $\frac{1}{4}$  million bits in one  $5\frac{1}{4}$ " high module
- Temperature range 0° to 50°C
- Non-volatile start up/shut down
- Power failure sensing and protection
- Front-access slide-out or vertical swing-out packaging
- Line drivers for all outputs
- Modular construction
- Output markers: data ready, memory busy, and end of cycle
- Self-contained cooling
- Wire-wrap connections for maximum reliability
- External clear for address and data register

The ICM-40 features 1 microsecond, full cycle operation plus access time of less than 500 nanoseconds — the first standard coincident-current integrated circuit core memory to offer this speed. The memory system is basically constructed with Computer Control Company, Inc.  $\mu$ -PAC monolithic integrated circuit modules, which provide almost  $\frac{1}{4}$  million bits of economical high-speed storage in a single compact  $5\frac{1}{4}$ " high unit. The modules, plus the application of a simplified accessing technique, result in a fast, versatile and reliable integrated circuit memory at a very low cost per bit.

The system is based on a three-wire, coincident-current magnetic core array. All logic, addressing, decoding, control, line driving and sensing functions utilize monolithic integrated circuitry. Production techniques proven in 3C's own facility (as well as those of other major manufacturers of integrated circuits) assure the highest level of quality control and environmental stability. The only active discrete components are the core stack selection switches and delay-line drivers. These components employ conservatively derated silicon semiconductors which operate well below their maximum ratings to assure long life and high reliability.

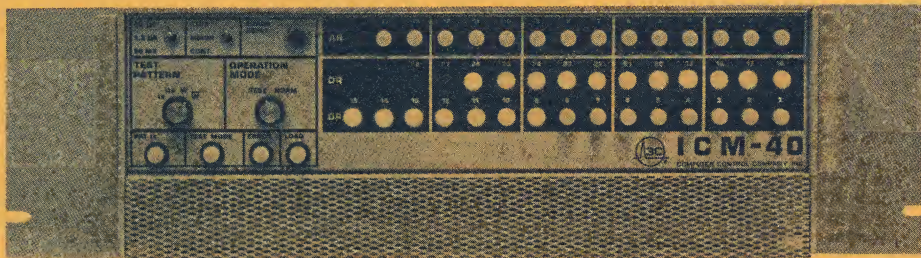
The small size of the ICM-40 does not sacrifice ease

of maintenance. All of the circuitry is packaged on readily accessible, removable, printed-circuit  $\mu$ -PAC modules. The ICM-40 system module is packaged in a  $5\frac{1}{4}$ " high unit designed to mount in a standard 24" deep, 19" equipment cabinet or rack. Maintenance, when required, is simplified since each memory unit is housed in a sliding-drawer which, when pulled out, tilts in several positions. The ICM-40 is also available in a housing designed for vertical mounting which swings clear of its rack for ready access to all internal components.

The ICM-40, when used in conjunction with the MP-40 power supply, is non-volatile on start up/shut down or power failure. Thus, no loss of information will occur when power is applied or removed or when a power failure occurs. The ICM-40 is also organized so that there is no necessity to normalize the system before operation.

As standard features, each ICM-40 memory is equipped with line drivers. The receiving and driving circuitry provides the memory with line noise immunity and impedance matching for twisted pair output cables. The memory is a self-contained system which includes address and data registers, internal delay-line timing and control, sense amplifiers, selection switches, and cooling.



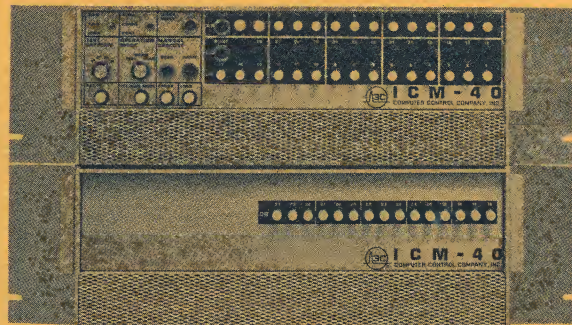


## NOW AVAILABLE

- 16,384 WORDS ..... 4-26 BITS
- 32,768 WORDS ..... 4-13 BITS
- PACKAGED IN ONE 5 1/4" HIGH UNIT

These larger capacity systems are offered in addition to 4096 word and 8192 word capacities.

# MULTIPLE UNIT SYSTEMS



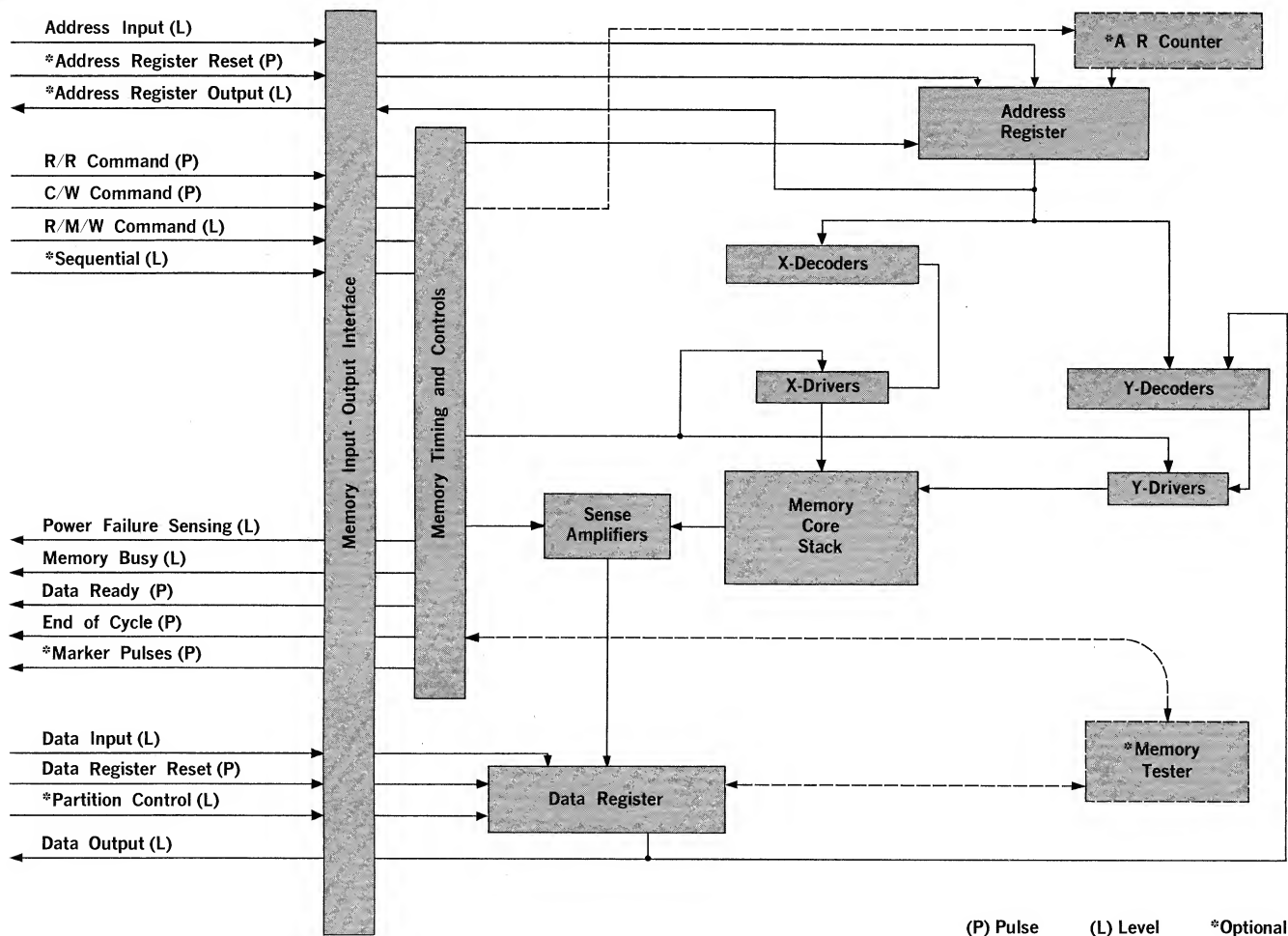
As illustrated, the ICM-40 Memory Modules may be stacked to further extend word size and/or capacity.

## A FEW ICM-40 FEATURES

- Wide operating temperature . . . 0°-50° C
- Adjustment free operation
- Information retention in case of power failure
- Self contained cooling

## EXTENSIVE USE OF INTEGRATED CIRCUITS PROVIDES:

- Savings in panel space
- Low power consumption
- Low spare parts cost
- Proven reliability



## basic elements

**Memory Timing and Control** accepts and interprets the input commands and provides the sequence of pulses needed to carry out the specific operation. Timing is derived using close-tolerance passive delay lines. In addition to the internal control signals, the timing circuitry generates the memory busy, data ready, and end of cycle output signals.

**Address Register** transfers the incoming address from the single-ended address input lines (or from the address counter during sequential operation) upon receipt of a clear/write or read/restore command. The address register stores this information until a new address and new cycle command are received. Outputs from the address register drive the selection switch decoding matrices.

**Selection** of a particular address is made by simultaneous excitation of the X and Y drive lines. Information from the address register is decoded to select one X line by a matrix of read/write selection switches and one Y line by a similar switch matrix. The selected combination of X and Y read/write switches allows a particular address to be accessed for reading from or writing into the core array. Y selection switches are decoded for each bit of the data word. During the

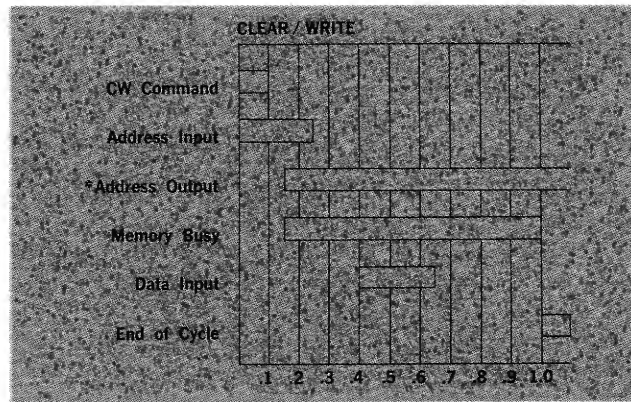
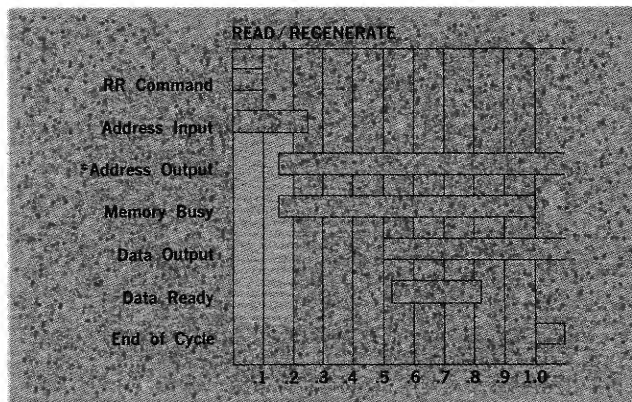
write or restore portion of a cycle, these Y switches control the data to be stored in the core array.

**Core Array** consists of a number of identical core planes and the associated diode matrices and bussing. The core planes are three-wire, coincident-current planes utilizing 30 mil ferrite cores. Sense windings in the planes link all of the addresses for a particular bit. Due to the logical organization of the system, inhibit windings are not required.

**Sense amplifiers** receive signals from the sense windings. They are monolithic integrated circuits that provide common-mode noise rejection, controlled signal amplification, threshold and time discrimination and pulse standardization. A sense winding, common to all addresses for a particular bit in the core array, detects the output signal from the selected core.

**Data Register** receives incoming data from single-ended input lines during a clear/write cycle. The outputs of the register control the Y selection switches to store the data in the core array. During a read/restore cycle, the outputs of the sense amplifiers are transferred to the data register, which staticizes the output until the next command pulse.





## operation

### INPUT SIGNALS

All inputs to the memory terminate in diode-coupled transistor (DTL) inverters. The use of DTL inverters guarantees a high noise immunity and stability. Thus, the length of communicating lines to the memory, even in a noisy system environment, becomes a less critical factor in memory operation. The resulting noise protection of the input gates is nominally 1.2 volts. Since circuitry is DC coupled, rise and fall time specifications also become less important.

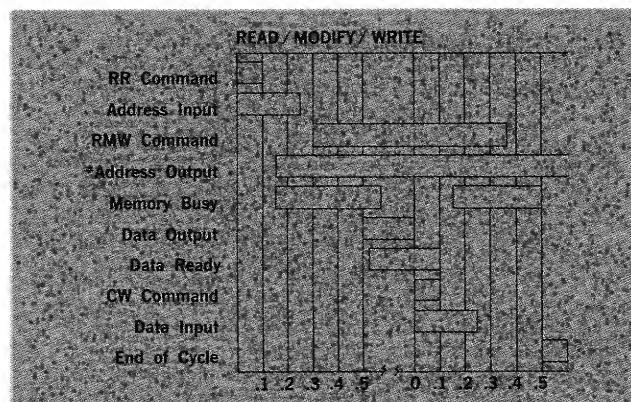
a. **Address-Register Inputs** are entered one line per bit, with a logical "ONE" input of +3.0 to +6.5 volts to set the corresponding address-register flip-flop. Address register inputs must be present and stable before the read/restore or clear/write pulse rises to 10% of its value. They must remain stable for at least 250 nanoseconds after the 90% point of the read/restore or clear/write pulse leading edge.

b. **Data-Register Input** signals must be stable no later than 400 nanoseconds after the initiation of a clear/write command. They must remain stable for the next 250 nanoseconds of the cycle.

c. **Read Regenerate Command (R/R)** is an input pulse (negative going), the leading edge of which initiates the read/restore memory cycle. This command must remain at 0 volts for at least 100 nanoseconds.

d. **Clear/Write Command (C/W)** is an input pulse (negative going), the leading edge of which initiates a clear/write memory cycle. This command must remain at 0 volts for at least 100 nanoseconds.

e. **Read/Modify/Write Command (R/M/W)** is an input level which, when asserted within 300 nanoseconds after a read/restore command, causes the cycle to terminate following data read-out. If this level is maintained and a subsequent clear/write pulse is furnished, the memory will write into the



\*STANDARD OPTION

address previously read, data provided on the information input lines, thus completing the read/modify/write operation.

### OUTPUT SIGNALS

All output signals from the memory are transmitted via cable drivers equipped with a unique short-circuit-protection network to prevent circuit damage due to accidental grounding of the output. These cable drivers are series terminated at the source to match twisted pair characteristic impedances between 50 and 100 ohms. They are capable of driving up to 10 feet of twisted pair cable. Loading at the receiving end should exceed 1000 ohms for reliable operation.

a. **Data Outputs** from the information register flip-flops are wired to cable-driver circuits. Data access time is equal to or less than 0.5 microseconds.

b. **Memory Busy** signal level rises 150 nanoseconds after the initiation of either a read/restore or clear/write and remains static until the end of cycle signal is generated.

c. **Data Ready** output signal indicates when information is available at the output interface and has a minimum duration of 300 nanoseconds. The signal is generated immediately after the transition of the information register output.

d. **End of Cycle** signal has a duration of 300 nanoseconds and reaches its final value immediately after the completion of the memory cycle.

## options

### specifications

**Memory Capacity:** 4,096 words 4-28 bits  
8,192 words 4-28 bits  
16,384 words 4-14 bits  
Multiple module capability allows the ICM-40 to be expanded to larger word size or capacity.

**Operating speed:** 1.0 microsecond for C/W and R/R  
1.25 microseconds for R/M/W

**Access time:** <0.5 microseconds

#### Logic levels (Input):

ZERO 0.0 volts to +1.0 volts  
ONE +3.0 to +6.5 volts

#### Logic levels (Output):

ZERO 0.0 volts to +0.40 volts  
ONE +4.0 volts to +6.5 volts

#### Output drive

**capability:** 10 feet of twisted pair cable

**Power:** 115 or 230 volts ( $\pm 15\%$ )  
50 or 60 cps ( $\pm 1$  cps)

#### Physical characteristics:

Height: 51¼"  
Width: 19"  
Depth: 22"  
Weight: <45 lbs.

#### Environment:

Operating temp 0° to 50°C

Non-operating temp -25°C to +80°C

Humidity 95% without condensation

Shock and vibration normal shipping conditions

1. **Sequential Addressing** is provided by the addition of a separate counter which supplies the address register with a sequenced address on command. The address is provided to the address register at the beginning of each sequential operation. The counter is incremented to the next address while the memory is performing the operating cycle.

2. **Memory Clear** provides a means of clearing all memory locations by asserting the sequential control line, the read/restore line and the read/modify/write line. All three levels must be held asserted for a period determined by the number of words stored in the memory. This option is provided in all memories equipped with the sequential address register option.

3. **Partitioning** allows the data register to be divided into two, three, or four independently controllable groups. This permits a selected portion of the data word to be changed without altering or destroying the rest of the word. Cycle time is not extended during this operation. Partitioning control levels must be stable no later than 50 nanoseconds after the initiation of a cycle command and must remain stable until 950 nanoseconds.

4. **Memory Tester** unit which is built into the ICM-40 is offered as a standard option. The tester includes a pattern generator capable of producing four fixed patterns, which are selected by a front-panel switch. These patterns include all "ONES", all "ZEROS", worst-case pattern, and worst-pattern complement. The tester loads the selected pattern into the memory and checks this pattern for accuracy during unload. If an error should occur, the test cycle will be interrupted and will indicate the address of the error and the data register bit that is in error. If desired, the tester controls may be set to allow test cycles to be continued in the presence of an error.

5. **Indicators** are individual display lamps for each of the address register and data register flip-flops. Other control flip-flops may be displayed to indicate the operating mode or condition of the memory.

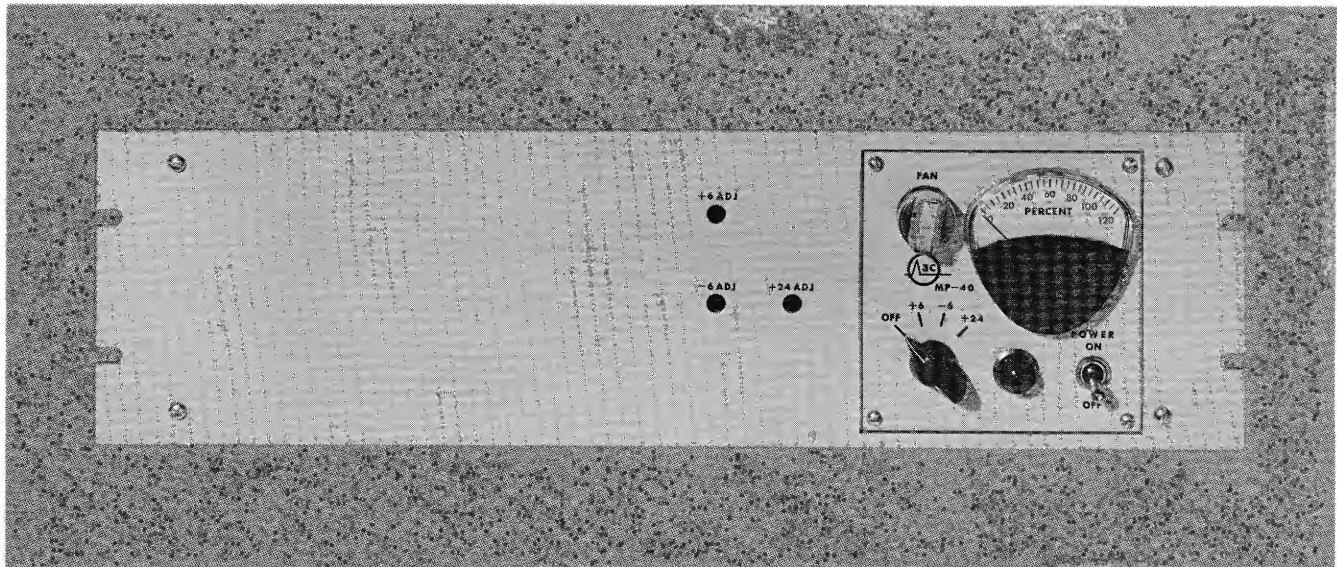
6. **Address Register Outputs** are single-ended levels which reach their significant transitions approximately 200 nanoseconds after either the R/R or C/W signals.

7. **Marker Pulses** (1 to 4) can be made available at specified times during memory cycles.

8. **Address Register Reset** is an input pulse (minimum width 100 nsec.). Assertion of this pulse resets the address counter which supplies the address register when operating in a sequential mode.

9. **Data Register Reset** is an input pulse. When the pulse is applied, it resets the data register.

## power supply model MP-40



The Model MP-40 power supply is a separate rack-mountable unit which has a panel height of  $5\frac{1}{4}$ ". The supply provides sufficient power for 28-bit ICM-40 memories of capacities up to 16,384 words. The supply has built-in power-failure sensing and protection. This provision assures no loss of information in the memory due to power turn-on, turn-off or failure. If desired, an optional voltmeter may be installed on the supply front panel. The MP-40 supply utilizes all-silicon semiconductors and features overload, line-transient, over-voltage, and thermal protection. It also has a temperature-compensated drive voltage.

This supply is available in two models:

1. Model MP-40, which operates from input power of 115 or 230 volts AC ( $\pm 15\%$ ) at 60 cps.
2. Model MP-40E, which is designed to accept an input voltage of 115 or 230 volts AC ( $\pm 15\%$ ) at 50 cps.

Environmental operating temperature range is  $0^{\circ}\text{C}$  to  $+60^{\circ}\text{C}$  with a storage temperature of  $-25^{\circ}\text{C}$  to  $+80^{\circ}\text{C}$ .

Overall dimensions:    Height —  $5\frac{1}{4}$ "  
                                 Width — 19"  
                                 Depth —  $17\frac{1}{4}$ "  
Weight:                      60 lbs.



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## 3C warranty

a) Computer Control Company, Inc. warrants all 3C instrument products against defects in workmanship, materials and construction under normal use and service for a period of ONE YEAR from the date of shipment, except that liability for semiconductors, switches, and potentiometers shall conform and be limited to the obligation of the original manufacturers' warranties covering these components.

b) This warranty does not extend to any of our products which have been subjected to misuse, neglect, accident, or improper installation or application. Nor shall it extend to products which have been repaired or altered outside of our factory.

c) For service under this warranty, please advise the factory promptly of all pertinent details. Transportation charges covering return of defective products to our factory shall be at our expense if such products are determined to be defective within the limitations of this warranty. Computer Control Company, Inc. will repair or replace the defective product in accordance with its own best judgment.

d) Computer Control Company, Inc. requests immediate notification of any claims arising from damage in transit in order to determine if carrier responsibility exists.

## other 3C products and services

A major area of 3C specialization is the design, development and manufacture of general purpose digital computers and special purpose systems.

3C is also a leading supplier of digital logic modules, pulse current generators and digital program generators.





COMPUTER CONTROL COMPANY, INC.